REMARKS

Status of Claims:

Claims 1-78 are pending in the application. Each of the pending claims defines an invention that is novel and unobvious over the cited art. Favorable consideration of this case is respectfully requested.

Summary of the Present Invention:

The present invention relates to parallel assembly technologies for fabricating multi-layer electronic interconnect structures having vias only between the layers being connected. The present invention provides that the vias of a first subassembly are electrically and mechanically connected to the circuitry of an adjacent subassembly by means of metallurgical bonds.

Rejections Under 35 U.S.C. § 112, 2nd Paragraph:

Claims 1-45 were rejected under 35 U.S.C. § 112, 2nd Paragraph, as being indefinite.

The Examiner cited claim 1 as being unclear. Claim 1 is hereby amended to recite: "facing said dielectric layer" as suggested by the Examiner.

Rejection Under 35 U.S.C. § 102(b):

Claims 1-3, 7-10, 12-14, 16-18, 20-21, 37-42, 45-48, 51-53, and 63-68 were rejected under 35 U.S.C. § 102(b) as being anticipated by Takenouchi (5,744,758).

Rejection under 35 U.S.C. § 102 requires the prior art disclose each and every limitation of the claimed invention (MPEP § 706.02). In determining anticipation, no claim limitation may be ignored. See *Pac-Tex, Inc. v. Amerace Corp.*, 14 USPQ2d 1871 (Fed. Cir. 1990). Anticipation requires the disclosure, in a prior art reference, of each and every recitation as set forth in the claims. See *Titanium Metals Corp. v. Banner*, 227 USPQ 773 (Fed. Cir 1985), *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 1 USPQ2d 1081 (Fed. Cir 1986), and *Akzo N.V. v. U.S. International Trade Commissioner*, 1 USPQ2d 1241 (Fed. Cir 1986). There must be no difference between the claimed invention and reference disclosure for an anticipation rejection under 35 U.S.C. § 102. See *Scripps Clinic and Research Foundation v. Genentech, Inc.*, 18 USPQ2d 1001 (CAFC 1991) and *Studiengesellschaft Kohle GmbH v. Dart Industries*, 220 USPQ 841 (CAFC 1984).

Claims 1, 37, 46, and 66-68 are hereby amended to recite formation of a metallurgical bond between the conductive materials in the vias of a first subassembly and the circuitry of an adjacent subassembly. The recitation of metallurgical bonding is incorporated into each of the claims in view of the dependence of the remaining claims on one of the amended claims. Metallurgical bonding was disclosed in the original specification at page 8, lines 13-16 and page 27, lines 2-16.

The evidentiary record fails to teach each limitation of the present invention in view of the silence of Takenouchi regarding forming metallurgical bonds. The present invention and Takenouchi teach filling vias with conductive paste. However, the present invention further teaches processing the paste so as to form metallurgical bonds. Takenouchi merely teaches conductive paste bonding and is silent as to the further process steps required to form metallurgical bonds.

Rejection Under 35 U.S.C. § 103(a):

Claims 4-6, 11, 15, 19, 24-33, 35-36, 49-50, 54-58, and 60-63 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Takenouchi in view of Lake (4,915,983).

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka.* All words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson.* (MPEP § 2143.03). When evaluating the scope of a claim, every limitation in the claim must be considered. See e.g. *In re Ochiai.* (MPEP § 2144.08). The evidentiary record fails to teach each limitation of the present invention.

Specifically, as discussed above, Takenouchi is silent as to metallurgical bonding. Lake fails to complete Takenouchi because Lake is similarly silent.

Claims 22-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Takenouchi in view of Arndt (3,601,523). Arndt was cited as providing a conductive paste applied with a squeegee. Arndt does not provide the teachings of the present invention, missing from Takenouchi because Arndt merely teaches conductive paste bonding and is silent as to the processing necessary to form metallurgical bonds.

Claims 34 and 59 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Takenouchi in view of Dishon (4,921,157). Dishon is silent as to metallurgical bonding so therefore fails to complete Takenouchi.

Claims 37-44 and 69-78 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Takenouchi in view of Pepe (5,635,010). Pepe is silent as to metallurgical bonding so therefore fails to complete Takenouchi.

None of the art cited by the Examiner teaches metallurgical bonding. Therefore, none of the cited art, whether taken severally or in any combination, anticipates or renders obvious the present invention.

Claim Objections:

Claims 13-15 were objected to as not further limiting claim 1.

Claim 1 provides, in pertinent part, a layered structure comprising a dielectric layer and a layer of a conductive material (metal) applied to one side of the dielectric layer. Claim 1 is directed to each of the ways in which such a structure may be made.

In a first, preferred method, a free-standing metal foil is laminated to a free standing, self supporting, dielectric layer.

In a second method a metal layer is deposited onto a free standing, self supporting, dielectric layer. Deposition can be by plating (electroless and/or electrolytic), vacuum deposition (sputtering or evaporation), chemical vapor deposition, and possibly others. In this case the metal is never in a free-standing form.

In a third method a dielectric layer is deposited onto a free standing metal foil. In this method the starting dielectric is provided as a liquid, or powder, that is applied and subsequently cured. An example would be a liquid polyimide precursor resin.

Claim 13 is directed at the third option and further limits claim 1 because claims 13 does not cover either of the first or second options.

Conclusion:

In view of the above, consideration and allowance are, therefore, respectfully solicited.

Accordingly, it is respectfully requested that the foregoing amendments be entered, that the application as so amended receive an examination on the merits, and that the claims as now presented receive an early allowance.

In the event the Examiner believes an interview might serve to advance the prosecution of this application in any way, the undersigned attorney is available at the telephone number noted below.

The Commissioner is hereby authorized to charge any fees or credit any overpayment associated with this communication, including any extension fees or fees for the net addition of claims, to Deposit Account No. 22-0185.

Respectfully submitted,

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APPENDIX

Kindly amend the claims as follows:

1. A parallel joining technology method for making a multi-layer electronic structure, the method comprising:

providing a plurality of sub-composites, wherein each said sub-composite is formed by the steps of

providing a layer of dielectric material having a first surface and a second surface, wherein said first surface is selected from the group consisting of a top surface and a bottom surface,

providing a layer of electrically conducting material on said first surface;

forming at least one blind via comprising a passage from said second surface through said dielectric layer to expose said layer of electrically conducting material facing said dielectric layer;

depositing electrically conducting material in at least one of said blind vias wherein said electrically conducting layer is in electrical contact with said electrically conductive material in said at least one blind via;

removing portions of the layer of electrically conducting material to define a pattern of circuitry;

stacking a plurality of said sub-composites;

aligning said plurality of sub-composites;

joining said plurality of sub-composites such that the electrically conducting material in at least one of said blind vias makes electrical contact by forming a metallurgical bond to [with] the conductive pattern on an adjacent sub-composite; and

filling spaces between adjacent sub-composites with electrically insulating material.

21. The method according to claim [21] 20, wherein the electrically conducting material is deposited in at least one of the at least one passage through the dielectric layer by plating and the plating is electroplating or electroless plating.

37. The method according to claim 1, wherein forming a metalurgical bond [joining the structures] comprises heating the structures to a temperature above a melting point of at least one

of the constituent [metals] of, or the cap deposited on, the electrically conducting material deposited in the at least one passage in the dielectric layer.

46. A parallel joining technology multi-layer electronic structure, comprising:

at least two substructures joined together, each substructure comprising a layer of dielectric material having a top surface and a bottom surface, a pattern of circuitry on one of the top surface [and] or the bottom surface of the layer of dielectric material, and at least one passage through the dielectric layer in connection with the circuitry, the at least one passage being filled with electrically conductive material, the at least two substructures being stacked on each other such that one of the electrically conducting material filling the at least one passage and the circuitry pattern on one substructure contacts and is electrically conductively joined by means of a metallurgical bond to one of the electrically conductive material filling the at least one passage and the circuitry pattern on another substructure; and

electrically insulating material substantially filling a space between facing substructures except between a joined filled passage and circuitry pattern.

66. A parallel joining technology [An] electronic package, comprising:

a multi-layer structure comprising at least two prefabricated substructures joined together, each substructure comprising a layer of dielectric material having a top surface and a bottom surface, a pattern of circuitry on one of the top surface and the bottom surface of the layer of dielectric material, and at least one passage through the dielectric layer in connection with the circuitry, the at least one passage being filled with electrically conducting material, the at least two substructures being stacked on each other such that one of the electrically conducing material filling the at least one passage and the circuitry pattern on one substructure contacts and is electrically conductively joined by a metallurgical bond to one of the electrically conducting material filling the at least one passage and the circuitry pattern on another substructure; and electrically insulating material between facing substructures except between a joined filled passage and a circuitry pattern; and a semiconductor chip attached to the multi-layer structure.

67. (Amended) A parallel joining technology [An] electronic package, comprising:

a printed wiring board comprising at least two prefabricated substructures joined together, each substructure comprising a layer of dielectric material having a top surface and a

bottom surface, a pattern of circuitry on one of the top surface and the bottom surface of the layer of dielectric material, and at least one passage through the dielectric layer in connection with the circuitry, the at least one passage being filled with electrically conducting material, the at least two substructures being stacked on each other such that one of the electrically conducting material filling the at least one passage and the circuitry pattern on one substructure contacts and is electrically conductively joined by a metallurgical bond to one of the electrically conducting material filling the at least one passage and the circuitry pattern on another substructure; and electrically insulating material between facing substructures except between a joined filled passage and a circuitry pattern; and

a plurality of electronic components attached to the printed wiring board.

68. A parallel joining technology method for making a multi -layer electronic interconnect structure, the method comprising:

providing a layer of dielectric material bonded to a layer of electrically conductive material, the layer of dielectric material having substantially uniform thickness;

forming at least one passage through the layer of dielectric material to expose a portion of the layer of electrically conductive material;

depositing electrically conducting material in at least one of the at least one passage through the layer of dielectric material, such that the electrically conducting material in the at least one passage is in electrical contact with the layer of electrically conducting material bonded to the layer of dielectric material and extends beyond a surface of the layer of dielectric material;

removing portions of the layer of electrically conducting material to define a pattern of circuit conductors, such that at least one of the circuit conductors remains electrically connected to the electrically conductive material deposited in that at least one of the at least one passage through the layer of dielectric material;

stacking and aligning a plurality of structures comprising the layer of dielectric material with circuit conductors disposed thereon and conductively filled passages therethrough such that one of the following conditions exists:

a) at least one conductively filled passage in a structure contacts at least one circuit conductor on the conductive layer of an adjacent structure,

b) at least one circuit conductor on the conductive layer of a structure contacts at least one conductively filled passage in an adjacent structure, or

c) at least one conductively filled passage in a structure contacts at least one conductively [fined] filed passage in an adjacent structure;

forming a metallurgical bond thereby electrically and mechanically joining the electrically conductive material filled one of the at least one passage that is aligned with an electrically conductive feature on an adjacent structure to the adjacent structure conductive features; and

filling spaces between the adjacent structures with an electrically insulating material.